Implementation of “Wilkinson Power Divider” on AWR Microwave Office

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Objective

• Design a Wilkinson power divider for 3GHz application with 1:2 power division ratio and implement on microstrip substrate of Permittivity: $\varepsilon_r=4.4$, Height of the substrate $H=1.6\text{mm}$, Conductor Thickness $T=0.05\text{mm}$, Loss tangent $\tan \delta = 0.001$.

• Steps to be followed:
  – Design the power divider for the power division ratio $K^2$ using design formula.
  – Calculate the Physical length and width of each microstrip line
  – Construct circuit and measure the performance parameters such as Input Return loss (dB:$S_{11}$), Insertion loss to port – 2 (dB:$S_{21}$), Insertion loss to port – 3 (dB:$S_{31}$), Isolation between two output ports (dB:$S_{32}$).
Here: $K^2 = 1/2 = 0.5$, therefore;

$$Z_{03} = Z_0 \sqrt{1 + K^2}$$

$$Z_{02} = Z_{03} K^2 = Z_0 \sqrt{K (1 + k^2)}$$

$$R = Z_0 K + \frac{1}{K}$$

$$R_2 = Z_0 K$$

$$R_3 = Z_0 / K$$

\[
\begin{align*}
Z_{03} &= 103.01 \Omega \\
Z_{02} &= 51.49 \Omega \\
R &= 106.08 \Omega \\
R_2 &= 35.35 \Omega \\
R_3 &= 70.72 \Omega 
\end{align*}
\]
Design of Wilkinson power divider

After placing microstrip lines, add resistance “RES” from “Element browser → Lumped Element”. For rotation – right click after drag the element.
Update the values of each element. Particularly, the output resistance $R_2$, $R_3$ are loads which can be included in Port-2 and Port-3 respectively. It is not advisable to use explicit resistance load at output side.
After created a new graph, include measurements from the Proper source name. Include $S_{11}$, $S_{21}$, $S_{31}$, $S_{32}$. 
Directly you can click “lighting button” in the toolbar for simulation.
Duplicate the rectangular graph to tabular, and write down the values.

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>DB(S(1,1))</th>
<th>DB(S(2,1))</th>
<th>DB(S(3,1))</th>
<th>DB(S(3,2))</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>-11.703</td>
<td>-2.0776</td>
<td>-5.1074</td>
<td>-11.37</td>
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<tr>
<td>2.4</td>
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<td>-5.0151</td>
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<td>2.8</td>
<td>-15.37</td>
<td>-1.9076</td>
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<tr>
<td>3.2</td>
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<td>3.6</td>
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<td>-1.8013</td>
<td>-4.8173</td>
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<td>4</td>
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<td>-1.7884</td>
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<tr>
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<td>-1.8079</td>
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<tr>
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<td>6</td>
<td>-11.278</td>
<td>-2.132</td>
<td>-5.1621</td>
<td>-11.174</td>
</tr>
</tbody>
</table>
Conclusion

1. At design frequency $f_o$, $S_{11} \sim 64\text{dB}$, which shows almost matched.

2. At design frequency $f_o$, $S_{21} = S_{12}$ and $S_{31} = S_{13}$ which shows that the WPD is a reciprocal network.

3. At design frequency $f_o$, Anti-log of (dB: $S_{21}$~dB:$S_{31}$) is $K^2$. Anti-log (-1.7884dB ~ (-4.8019dB) = -3.01dB) = 0.5 which shows the design is correct and better performance is obtained.

4. Isolation 64.54dB ($S_{32}$), which shows that two output port are isolated each other and no signal transfer between them. This is useful for lossless property.